REMARKS

Applicants have carefully reviewed and considered the Office Action mailed on January 25, 2006, and the references cited therewith.

Claims 4, 7, 11, 17, 22-24, 28, 32 and 39 have been amended to address matters form. No claims have been canceled or added. Claims 1-44 remain pending in the present application.

Claim Rejections – 35 U.S.C. § 103

Rejections on Edwards in view of Mirsky

In the Office action, the Examiner rejected claims 1, 3-22, 24-44 under 35 U.S.C. § 103(a) as being obvious over Edwards, et al., "Hardware/Software Partitioning For Performance Enhancement", 1995, Partitioning Hard-ware-Software Codesigns, IEEE Colloquium (hereafter "Edwards") in view of U.S. Patent 5,915,123 to Mirsky et al. (hereafter "Mirsky") Applicants respectfully traverse this rejection.

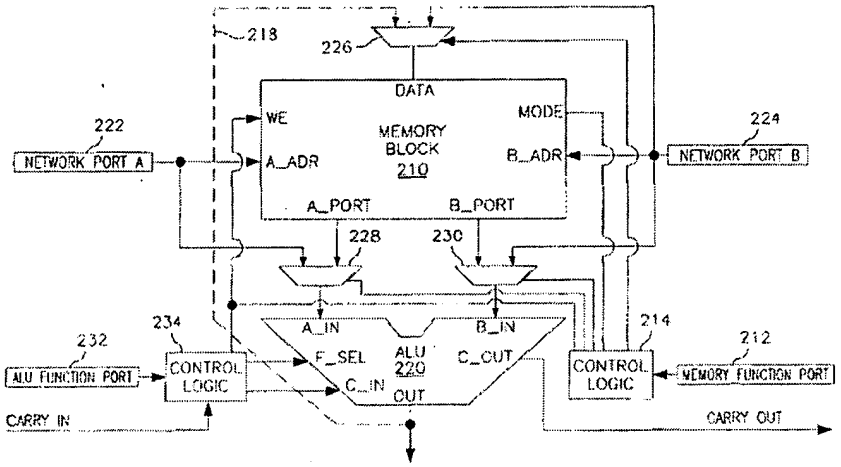
Claim 1 recites:

> A method of creating run time executable code for a processing element array, comprising:
> partitioning the processing element array into a plurality of hardware accelerators;
> identifying a plurality of functions in a program source code that are anticipated to consume a substantial execution time;
> decomposing the program source code into a plurality of kernel sections, wherein the identified plurality of functions are recognized as the plurality of kernel sections;
> mapping said plurality of kernel sections into a plurality of hardware dependent executable code for execution on the plurality of hardware accelerators; and
> forming a matrix describing different combinations of said plurality of hardware accelerators, code variants and said hardware dependent executable code to support run time execution of the plurality of kernel sections by the processing element array, wherein each code variant performs a function whose inputs and outputs are identical.

It is well settled that in order to establish a *prima facie* case of obviousness, the Examiner must establish that the cited references, when combined, disclose or suggest each of the elements of a rejected claim. Applicants respectfully submit that the suggested combination of Edwards and Mirsky fails to disclose or suggest each of the elements of claim 1.

Claim 1 is directed to a method of creating run time executable code for a processing element array. An example of such a processing array is illustrated in Figure 1 of the application. As described in the specification, such a processing element array may include an array of multiple context processing elements (MCPEs). An example of such an embodiment of an MCPE is illustrated in Figure 2 of the present application. For the Examiner's convenience, Figure 2 of the application is presented below.

FIG.2



As shown in Figure 2, a processing element may include a memory block 210 and an arithmetic logic unit 220, as well as associated ports and control logic. As described on page 6, lines 12-18, individual MCPEs of a processing element array may be independently configured and controlled.

In the Office Action, the Examiner relies on Edwards as disclosing a processing element array and "partitioning the processing element array into a plurality of hardware accelerators." Specifically, the Examiner asserts that the field programmable gate array (FPGA) of Edwards discloses the processing element array of claim 1 and that Edwards discloses partitioning of the FPGA of Edwards into a plurality of hardware accelerators. Applicants respectfully submit that the Examiner's analysis of Edwards is incorrect, and that nothing in Mirsky serves to compensate for this deficiency of Edwards.

An FPGA is collection of individual logic gates, typically on an integrated circuit. The interconnections between the logic gates of such FPGAs are programmable (e.g., electrically selectable). The term FPGA is defined in the Modern Dictionary of Electronics, Seventh

Edition, Rudolf R. Graf © 1999 as "An array of gates on a chip whose interconnections can be arranged electronically by the user."

As is known, specific logic functions may be implemented in an FPGA by selectively programming the interconnects of an FPGA. As those working in this area at the time of the invention would have appreciated, the architecture and structure of an FPGA device is significantly different than that of a processing element array. While a processing element array includes an array of processing elements (e.g., MCPEs such as illustrated in FIG. 2 of the application), an FPGA, in comparison, merely consists of an array of individual gates which may be interconnected using electrically selectable interconnect points.

With respect to "partitioning the processing element array into a plurality of hardware accelerators," as recited in claim 1, the Examiner relies on Edwards disclosure of a system partitioner, page 2, ¶ 5 as constituting this element of claim 1. The system partitioner of Edwards is used to "translate C code to ... HardwareC code in order to enable high-level hardware synthesis" (to enable the translated code to be implemented in an FPGA). Edwards defines HardwareC on page 2, ¶ 5 as "a hardware description language that allows the behaviour of a digital system to be defined as a collection of concurrent processes which operate continuously." In the system of Edwards, the HardwareC code is used to configure the interconnects for an FPGA device. For instance, Edwards states on page 3, ¶ 2 that a "hardware synthesizer accepts the HardwareC code ... and produces the configuration data for a Xilinx 40XX FPGA." Applicants respectfully submit that the translation of C code in HardwareC code and the producing an FGPA configuration based on the HardwareC codes does not disclose or suggest "partitioning the processing element array into a plurality of hardware accelerators," as recited in claim 1.

Furthermore, because Edwards does not suggest, describe, disclose or even mention the use of a processing element array, or partitioning such a processing element array into a plurality of hardware accelerators, as is recited in claim 1, Edwards cannot disclose or suggest "mapping [a] plurality of kernel sections into a plurality of hardware dependent executable code for execution on the plurality of hardware accelerators", as is also recited in claim 1.

Additionally, in rejecting claim 1, the Examiner relied on Mirsky as disclosing "forming a matrix describing different combinations of said plurality of hardware accelerators, code

variants and said hardware dependent executable code to support run time execution of the plurality of kernel sections by the processing element array, wherein each code variant performs a function whose inputs and outputs are identical", as recited in claim 1. Mirsky is directed to a method and apparatus for providing local control of processing elements in a processing element array. *See* Abstract. Even assuming, for the sake of argument, that the Examiner's remarks with respect to Mirsky are correct, Applicants respectfully submit that one of skill working in this area would not have been motivated to combine the teachings of Edwards and Mirsky. As was discussed above, Edwards is directed to translating C code to HardwareC code and determining an FPGA configuration based on the HardwareC codes. Edwards does not disclose or suggest the use of a processing element array, as recited in claim 1. Because, as was noted above, the architectures and structures of FPGA devices and processing element arrays are substantially different, one of skill in the art would not be motivated to combine the subject matter of Edwards with the subject matter of Mirsky. In fact, because of the architectural differences between FPGA devices and processing element arrays, Applicants respectfully assert that the subject matter of Edwards is substantially technically incompatible with the subject matter of Mirsky.

Based on the foregoing, claim 1 is not obvious over Edwards in view of Mirsky. Therefore, Applicants respectfully request that the Examiner withdraw the rejection of claim 1.

Without addressing the merits of the Examiner's statements regarding claims 3-21, which are not conceded, Applicants point out that claims 3-21 depend ultimately from claim 1 and include all of its limitations and the limitations of any intervening claims, while adding further limitations. Thus, the arguments made above regarding claim 1 apply equally to claims 3-21 and are herein incorporated. Therefore, Applicants respectfully request that the Examiner withdraw the rejection of claims 3-21.

Independent claims 22, 43 and 44 include similar limitations to the limitations of claim 1 discussed above. Therefore, claims 22, 43 and 44 are not obvious over Edwards in view of Mirsky for at least the same or similar reasons as discussed above with respect to claim 1. Furthermore, claims 24-42 depend from claim 22 and are not obvious over Edwards in view of Mirsky on at least the same basis as claim 22. Applicants respectfully request that the Examiner withdraw the rejection of claims 22 and 23-44.

Rejections on Edwards in view of Mirsky and Tseng

Also in the Office Action, the Examiner has rejected claims 2 and 23 under 35 U.S.C. § 103 as being obvious over Edwards in view of Mirsky and further in view of U.S. Patent 6,009,256 to Tseng et al. (hereafter "Tseng"). Applicants respectfully address this rejection.

Claim 2 depends from claim 1 and claim 23 depends from claim 22. The Examiner relies on Tseng as disclosing partitioning into digital signal processors. Even assuming, merely for the sake of argument, that the Examiner's remarks regarding Tseng are correct, Tseng fails to make up for the deficiencies of Edwards and Mirsky discussed above with respect to claims 1 and 22. Therefore, claims 2 and 23 are not obvious over Mirsky on the same basis as discussed above with regard to their respective independent claims. Applicants respectfully request that the Examiner withdraw the rejection of claims 2 and 23.

Information Disclosure Statement

Further in the Office Action, the Examiner stated that the information disclosure statement (IDS) filed on November 12, 2004 does not appear to comply with 37 C.F.R. 1.98(a)(2). Specifically, the Examiner asserts that copies of the non-patent documents are not found.

Applicants are uncertain as to the reason for this assertion by the Examiner. The IDS of November 12, 2004 was merely a copy of the IDS that was originally filed in the present application on October 16, 2000. The non-patent references cited in that IDS were included with the October 16, 2000 submission. The Examiner indicated these non-patent documents as being considered in a signed and initialed PTO 1449 form that was included with the Office Action mailed on April 10, 2003. A courtesy copy of this signed and initialed 1449 form is being included along with this response.

Applicants do, however, note that a single U.S. Patent (5,956,518) was not initialed on the 1449 form of the October 16, 2000. Accordingly, Applicants would appreciate the Examiner returning a copy of the attached 1449 form indicating consideration of this U.S. Patent in addition to the other art cited, which was already indicated as being considered.

Conclusion

Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney (703-286-5735) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-3521.

Respectfully submitted,

Brake Hughes PLC
Customer Number 57426
703-286-5735

Date: June 26, 2006 By: _____
William G. Hughes
Reg. No. 46,112

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 26th day of June, 2006.

_____ _____
Shellie Bailey Signature